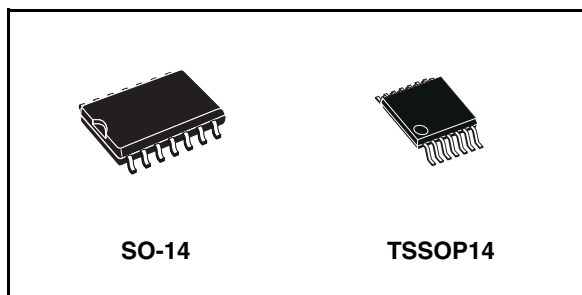


HEX SCHMITT inverter

Features

- High speed: $t_{PD} = 5.5\text{ns}$ (typ.) at $V_{CC} = 5\text{V}$
- Low power dissipation:
 $I_{CC} = 2\text{ }\mu\text{A}$ (Max.) at $T_A = 25^\circ\text{C}$
- Typical hysteresis: $V_h = 1\text{V}$ at $V_{CC} = 4.5\text{V}$
- Power down protection on inputs
- Symmetrical output impedance:
 $|I_{OH}| = I_{OL} = 8\text{ mA}$ (Min)
- Balanced propagation delays:
 $t_{PLH} \cong t_{PHL}$
- Operating voltage range:
- $V_{CC}(\text{Opr}) = 2\text{V to } 5.5\text{V}$
- Pin and function compatible with
74 series 14
- Improved latch-up immunity
- Low noise: $V_{OLP} = 0.8\text{V}$ (Max.)



Description

The 74VHC14 is an advanced high-speed CMOS HEX SCHMITT inverter fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

The internal circuit is composed of 3 stages including buffer output, which enables high noise immunity and stable output.

Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

Pin configuration and function are the same as those of the 74VHC04 but the 74VHC14 has hysteresis.

This together with its schmitt trigger function allows it to be used on line receivers with slow rise/fall input signals.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Table 1. Device summary

Part number	Package	Packaging
74VHC14MTR	SO-14	Tape and reel
74VHC14TTR	TSSOP14	Tape and reel

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1 Logic symbols and I/O equivalent circuit

Figure 1. IEC logic symbols

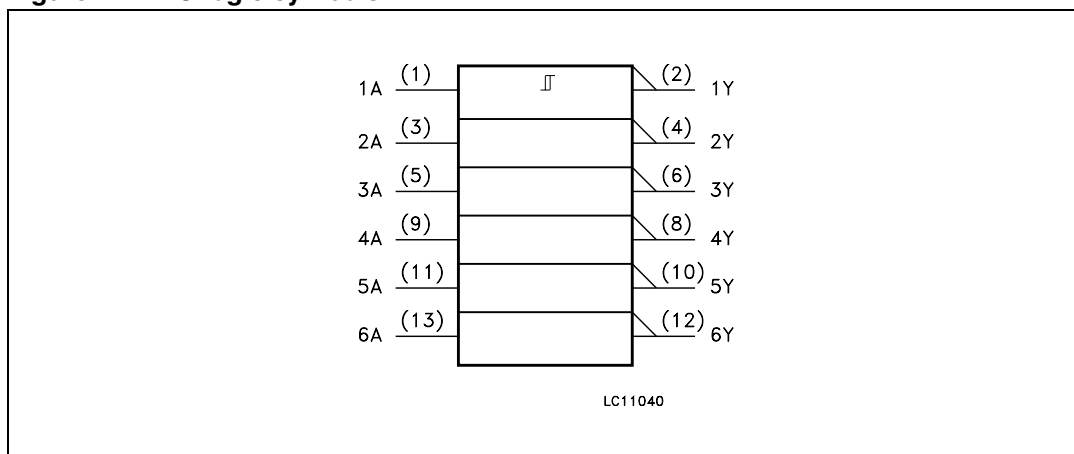
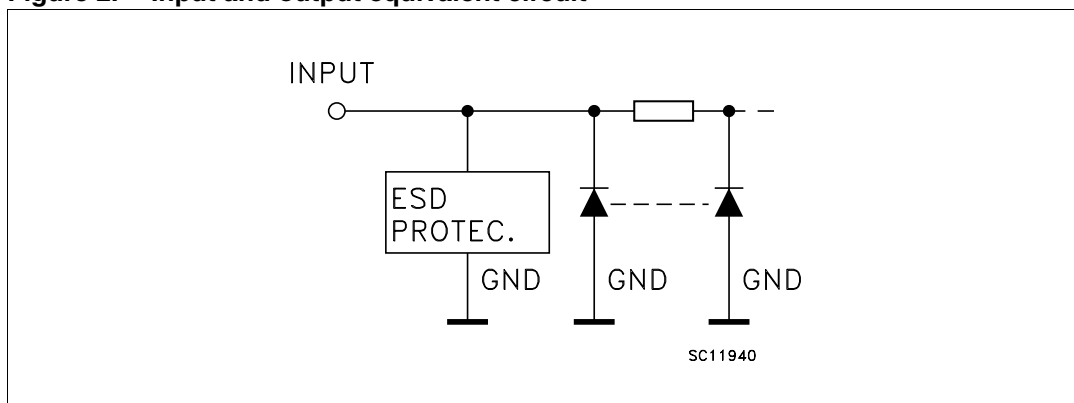


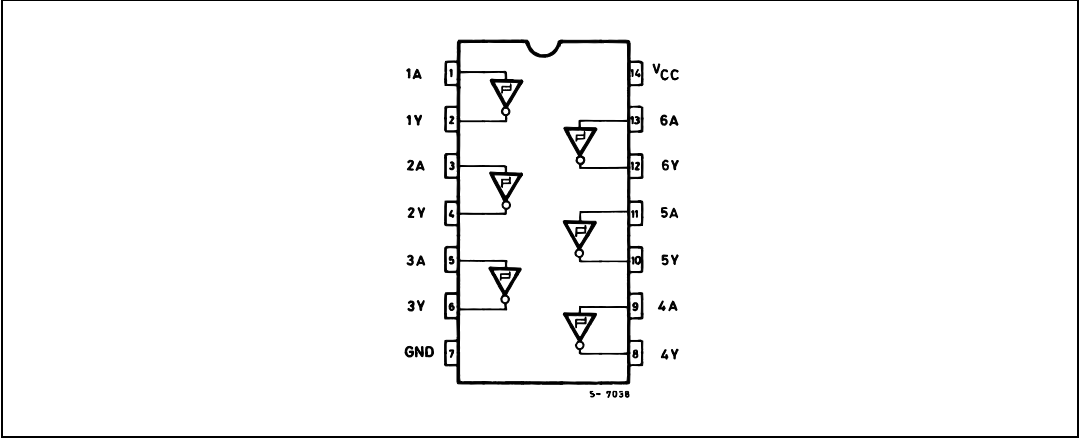
Figure 2. Input and output equivalent circuit



2 Pin settings

2.1 Pin connection

Figure 3. Pin connection (top through view)



2.2 Pin description

Table 1. Pin description

Pin N°	Symbol	Name and function
1, 3, 5, 9, 11, 13	1A to 6A	Data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	Data outputs
7	GND	Ground (0V)
14	V _{CC}	Positive supply voltage

2.3 Truth table

Table 2. Truth table

Inputs	Output
A	Y
L	H
H	L

3 Maximum rating

stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. these are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. exposure to absolute maximum rating conditions for extended periods may affect device reliability. refer also to the STMicroelectronics sure program and other relevant quality documents.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_I	DC input voltage	-0.5 to +7.0	V
V_O	DC output voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC input diode current	- 20	mA
I_{OK}	DC output diode current	± 20	mA
I_O	DC output current	± 25	mA
I_{CC}	DC supply current per supply pin	± 50	mA
I_{GND}	DC ground current per supply pin	± 50	mA
T_{stg}	Storage temperature	-65 to +150	°C
T_L	Lead temperature (10 sec)	300	°C

3.1 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2 to 5.5	V
V_I	Input voltage	0 to 5.5	V
V_O	Output voltage	0 to V_{CC}	V
T_{op}	Operating temperature	-55 to 125	°C

4 Electrical characteristics

Table 5. DC specifications

Symbol	Parameter	Test condition		Value							Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V _{t+}	High level threshold voltage	3.0				2.2		2.2		2.2	V
		4.5				3.15		3.15		3.15	
		5.5				3.85		3.85		3.85	
V _{t-}	Low level threshold voltage	3.0		0.9			0.9		0.9		V
		4.5		1.35			1.35		1.35		
		5.5		1.65			1.65		1.65		
V _h	Hysteresis voltage	3.0		0.3		1.2	0.3	1.2	0.3	1.2	V
		4.5		0.4		1.4	0.4	1.4	0.4	1.4	
		5.5		0.5		1.6	0.5	1.6	0.5	1.6	
V _{OH}	High level output voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		2.9		
		4.5	I _O =-50 μA	4.4	4.5		4.4		4.4		
		3.0	I _O =-4 mA	2.58			2.48		2.4		
		4.5	I _O =-8 mA	3.94			3.8		3.7		
V _{OL}	Low level output voltage	2.0	I _O =50 μA		0.0	0.1		0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1		0.1	
		4.5	I _O =50 μA		0.0	0.1		0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44		0.55	
		4.5	I _O =8 mA			0.36		0.44		0.55	
I _I	Input leakage current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent supply current	5.5	V _I = V _{CC} or GND			2		20		20	μA

Table 6. AC electrical characteristics (Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test condition			Value						Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
					Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation delay time	3.3 ⁽¹⁾	15			8.3	12.8	1.0	15.0	1.0	15.0	ns
		3.3 ⁽¹⁾	50			10.8	16.3	1.0	18.5	1.0	18.5	
		5.0 ⁽²⁾	15			5.5	8.6	1.0	10.0	1.0	10.0	
		5.0 ⁽²⁾	50			7.0	10.6	1.0	12.0	1.0	12.0	

1. Voltage range is $3.3\text{V} \pm 0.3\text{V}$ 2. Voltage range is $5.0\text{V} \pm 0.5\text{V}$ **Table 7. Capacitive characteristics**

Symbol	Parameter	Test condition	Value								Unit
			T _A = 25°C			-40 to 85°C		-55 to 125°C			
			Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
C _{IN}	Input capacitance			6	10		10		10	pF	
C _{PD}	Power dissipation capacitance ⁽¹⁾			14						pF	

1. C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation.
 $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/6$ (per gate)

Table 8. Dynamic switching characteristics

Symbol	Parameter	Test condition		Value								Unit
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C			
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
V _{OLP}	Dynamic low voltage quiet output ^{(1) (2)}	5.0	C _L = 50 pF		0.3	0.8					V	
V _{OLV}				-0.8	-0.3							
V _{IHD}	Dynamic high voltage input ^{(1) (3)}	5.0		3.5							V	
V _{ILD}	Dynamic low voltage input ^{(1) (3)}	5.0					1.5					V

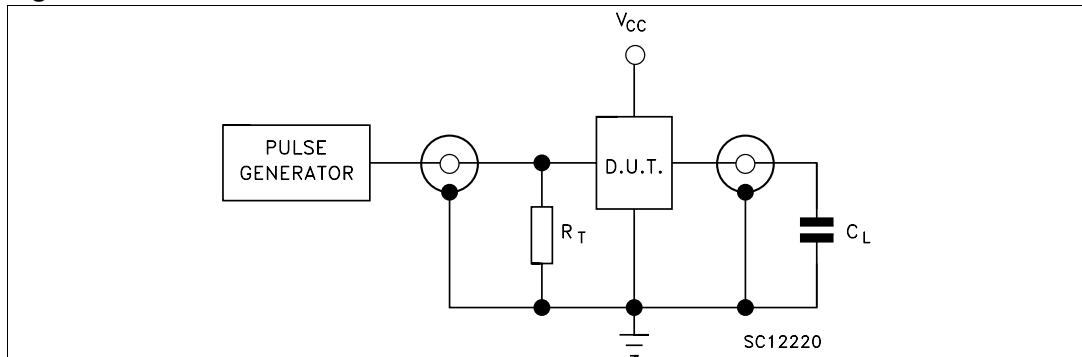
1. Worst case package.

2. Max number of outputs defined as (n). Data inputs are driven 0V to 5.0V, (n-1) outputs switching and one output at GND.

3. Max number of data inputs (n) switching. (n-1) switching 0V to 5.0V. Inputs under test switching: 5.0V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), $f = 1\text{MHz}$.

5 Test circuit

Figure 4. Test circuit

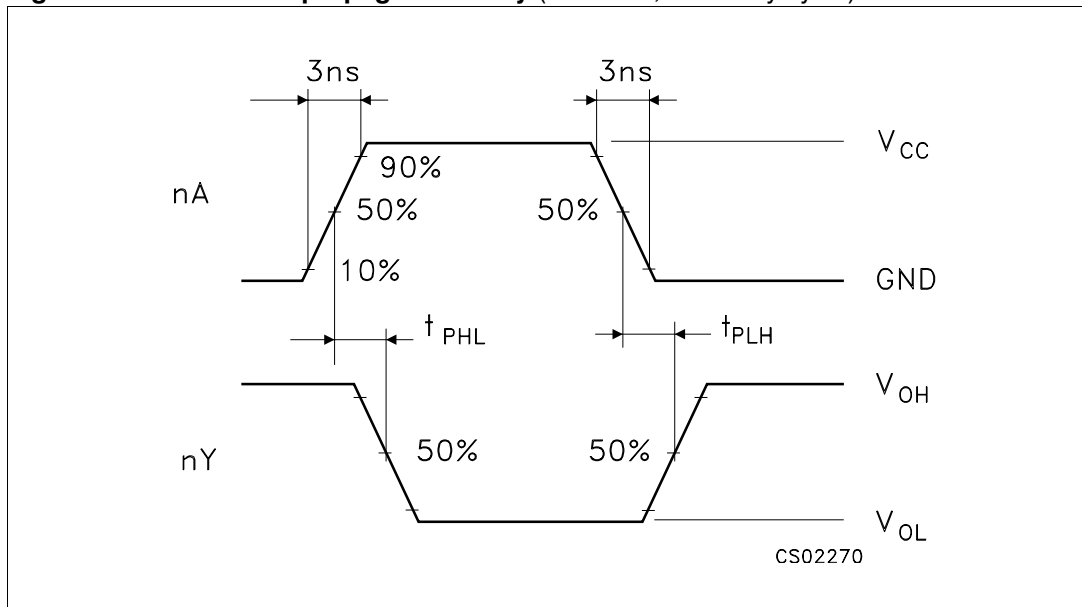


$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

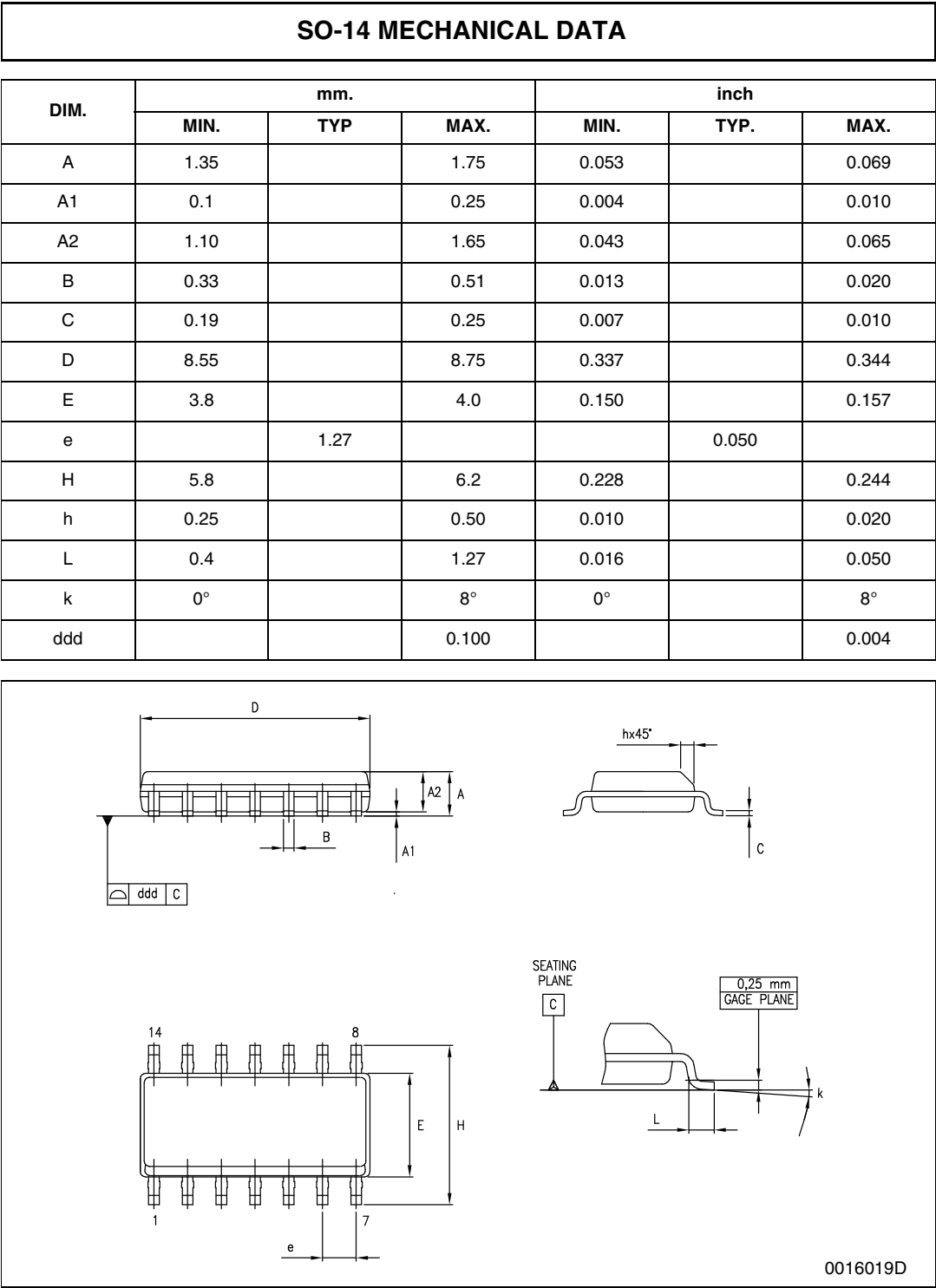
6 Waveforms

Figure 5. Waveform - propagation delay ($f = 1\text{MHz}$; 50% duty cycle)

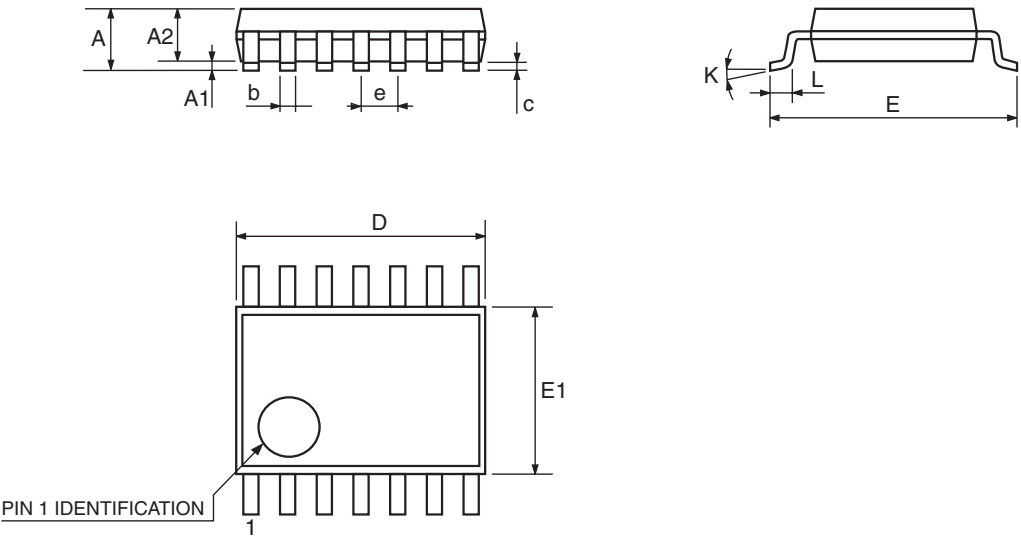


7 Package mechanical data

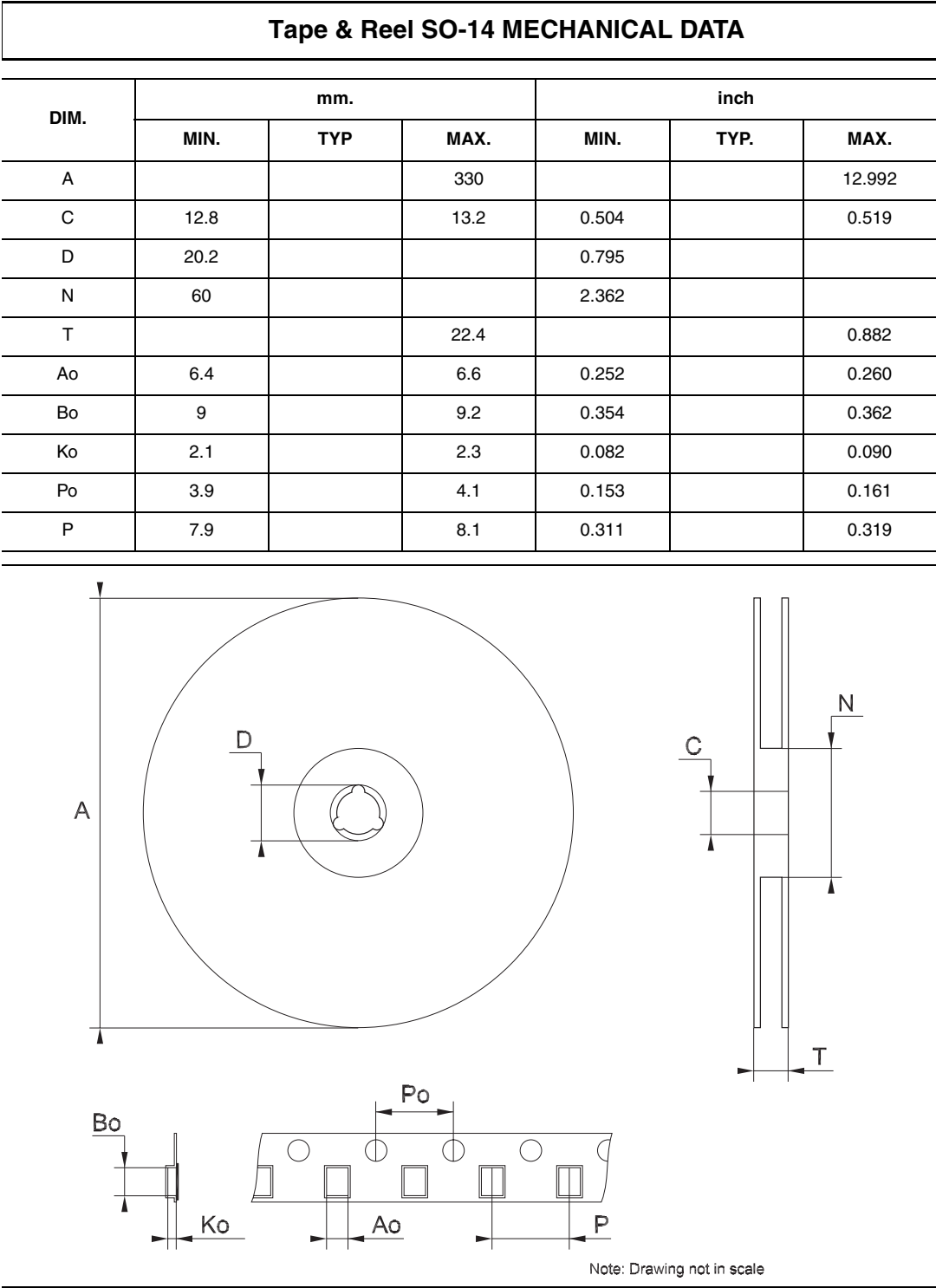
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



TSSOP14 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



0080337D



Tape & Reel TSSOP14 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.7		6.9	0.264		0.272
Bo	5.3		5.5	0.209		0.217
Ko	1.6		1.8	0.063		0.071
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319

The drawing includes three views of the TSSOP14 package. The top view shows a circular carrier with diameter A and a central hole with diameter D. The side view shows the package height N and the lead length C. The detail view shows the package width P, lead width Bo, lead thickness Ko, and the distance between leads Po and Ao.

Note: Drawing not in scale

8 Revision history

Table 9. Revision history

Date	Revision	Changes
12-Nov-2004	6	Ordering codes revision - pag. 1.
03-May-2007	7	Document reformatted, updated Table 5 on page 6

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